THAT WHICH IS CLAIMED IS:

1. An asynchronous data transmission device comprising:

a data reception terminal for receiving data including a synchronization signal;

a register connected to said data reception terminal for receiving the data being clocked by a sampling signal in synchronization with a local clock signal; and

a clock deviation measurement circuit connected to said register for determining a number M of periods of the sampling signal appearing during K periods of the synchronization signal, and for comparing the number M to a tolerance margin defined by a lower threshold and an upper threshold.

2. An asynchronous data transmission device according to Claim 1, wherein said clock deviation measurement circuit comprises:

deviation flag means for delivering a deviation flag having a first logic value when the number M is not between the lower and upper thresholds, and having a second logic value when the number M is between the lower and upper thresholds.

3. An asynchronous data transmission device according to Claim 1, wherein said clock deviation measurement circuit comprises:

first logic signal means for delivering a first logic signal having a first logic value when the number M of periods of the synchronization signal is equal to K;

second logic signal means for delivering a second logic signal having a second logic value when the number M of periods of the sampling signal is between the lower and upper thresholds; and

third logic signal means for delivering a third logic signal having a determined logic value when the first and second logic signals respectively have the first and second logic values.

4. An asynchronous data transmission device according to Claim 1, wherein said clock deviation measurement circuit determines the number M of periods of the sampling signal appearing between two rising edges of the synchronization signal or between two falling edges of the synchronization signal.

5. An asynchronous data transmission device according to Claim 4, wherein said clock deviation measurement circuit comprises detection means to verify that the detection of the rising edge or the falling edge corresponds to the reception of several samples of the synchronization signal having a logic majority value corresponding to the edge detected.

6. An asynchronous data transmission device according to Claim 1, wherein said clock deviation measurement circuit determines the number M of periods of the sampling signal appearing between a rising edge and a falling edge of the synchronization signal or between a falling edge and a rising edge of the synchronization signal.

7. An asynchronous data transmission device

according to Claim 6, wherein said clock deviation measurement circuit comprises verification means to verify that the detection of the rising edge or the falling edge corresponds to the reception of several samples of the synchronization signal having a logic majority value corresponding to the edge detected.

8. An asynchronous data transmission device according to Claim 1, wherein said clock deviation measurement circuit is configured as an integrated circuit.

9. An asynchronous data transmission device according to Claim 8, wherein said clock deviation measurement circuit comprises a plurality of logic gates, flip-flops, logic comparators and counters connected together.

10. An asynchronous data transmission device according to Claim 1, wherein the synchronization signal received by said data reception terminal includes a synchronization character; and further comprising a status machine connected to said register for detecting reception of the synchronization character and for activating said clock deviation measurement circuit when the synchronization character is detected.

11. A microcontroller comprising:

an asynchronous data transmission device comprising

a data reception terminal for receiving data including a synchronization signal,

a register connected to said data reception terminal for receiving the data being clocked by a sampling signal in synchronization with a local clock signal, and

a clock deviation measurement circuit connected to said register for determining a number M of periods of the sampling signal appearing during K periods of the synchronization signal, and for comparing the number M to a tolerance margin defined by a lower threshold and an upper threshold; and

a central unit connected to said asynchronous data transmission device for receiving the data.

12. A microcontroller according to Claim 11, wherein said clock deviation measurement circuit delivers a deviation flag having a first logic value when the number M is not between the lower and upper thresholds, and having a second logic value when the number M is between the lower and upper thresholds.

13. A microcontroller according to Claim 11, wherein said clock deviation measurement circuit comprises:

a first logic signal circuit for delivering a first logic signal having a first logic value when the number M of periods of the synchronization signal is equal to K;

a second logic signal circuit for delivering a second logic signal having a second logic value when the number M of periods of the sampling signal is

between the lower and upper thresholds; and

a third logic signal circuit for delivering a third logic signal having a determined logic value when the first and second logic signals respectively have the first and second logic values.

14. A microcontroller according to Claim 11, wherein said clock deviation measurement circuit determines the number M of periods of the sampling signal appearing between two rising edges of the synchronization signal or between two falling edges of the synchronization signal.

15. A microcontroller according to Claim 14, wherein said clock deviation measurement circuit verifies that the detection of the rising edge or the falling edge corresponds to the reception of several samples of the synchronization signal having a logic majority value corresponding to the edge detected.

16. A microcontroller according to Claim 11, wherein said clock deviation measurement circuit determines the number M of periods of the sampling signal appearing between a rising edge and a falling edge of the synchronization signal or between a falling edge and a rising edge of the synchronization signal.

17. A microcontroller according to Claim 16, wherein said clock deviation measurement circuit verifies that the detection of the rising edge or the falling edge corresponds to the reception of several samples of the synchronization signal having a logic majority value corresponding to the edge detected.

18. A microcontroller according to Claim 11, wherein the synchronization signal received by said data reception terminal includes a synchronization character; and wherein said asynchronous data transmission device further comprises a status machine connected to said register for detecting reception of the synchronization character, and for activating said clock deviation measurement circuit when the synchronization character is detected.

19. A method for transmitting asynchronous data comprising:

receiving data including a synchronization signal on a data reception terminal;

reading the data being clocked by a sampling signal in synchronization with a local clock signal; and

measuring deviation of the local clock signal by

determining a number M of periods of the sampling signal appearing during K periods of the synchronization signal, and

comparing the number M to a tolerance margin defined by a lower threshold and an upper threshold.

20. A method according to Claim 19, further comprising providing a deviation flag having a first logic value when the number M is not between the lower and upper thresholds, and having a second logic value when the number M is between the lower and upper thresholds.

21. A method according to Claim 19, further comprising:

providing a first logic signal having a first logic value when the number M of periods of the synchronization signal is equal to K;

providing a second logic signal having a second logic value when the number M of periods of the sampling signal is between the lower and upper thresholds; and

providing a third logic signal having a determined logic value when the first and the second logic signals respectively have the first and second logic values.

22. A method according to Claim 19, wherein the number M of periods of the sampling signal is determined between two rising edges of the synchronization signal or between two falling edges of the synchronization signal

23. A method according to Claim 22, further comprising verifying that the detection of the rising edge or the falling edge corresponds to the reception of several samples of the synchronization signal having a logic majority value corresponding to the edge detected.

24. A method according to Claim 19, wherein the number M of periods of the sampling signal is determined between a rising edge and a falling edge of the synchronization signal or between a falling edge and a rising edge of the synchronization signal.

25. A method according to Claim 24, further comprising verifying that the detection of the rising edge or the falling edge corresponds to the reception of several samples of the synchronization signal having a logic majority value corresponding to the edge detected.

26. A method according to Claim 19, wherein the synchronization signal received by the data reception terminal includes a synchronization character; wherein the reading comprises detecting reception of the synchronization character; and wherein the measuring is performed in response to the synchronization character being detected.

27. A method according to Claim 19, wherein the receiving, the reading and the measuring is implemented in an asynchronous data transmission device.